

## **METHOD AND SYSTEM TO DIFFERENTIALLY ENHANCE SENSOR DYNAMIC RANGE**

### **CROSS-REFERENCES TO RELATED APPLICATIONS**

[0001] Priority is claimed from applicant's U.S. Provisional Patent Application No. 60/462,167 filed on 11 April 2003 entitled "Differential Dynamic Range Enhancement Methods and Systems", assigned to Canesta, Inc., the entire content of which application is incorporated herein by reference.

### **FIELD OF THE INVENTION**

[0002] The invention relates generally to optical sensors, and more particularly to enhancing dynamic range of such sensors, while allowing the sensors to be fabricated using CMOS techniques.

### **BACKGROUND OF THE INVENTION**

[0003] Systems that rely upon sensing optical energy to discern information are known in the art and have many applications. Exemplary applications might include an optical-based system to determine range between the system and a target object, or to identify and recognize features of a target object. Many such systems acquire two-dimensional or intensity-based information, and rely upon an intensity image of light reflected from a target object. Such luminosity-based systems can use ambient light falling upon the target object, or may actively generate light that is directed toward the target object.

[0004] Unfortunately, it is difficult to accurately determine distance solely from the amplitude and brightness of an intensity image. For example, in a range finding system, a highly reflecting target object that is father away from the system can produce a greater amplitude signal than a nearer target object that is less reflective. The result would be that the more distant, shiny, object is erroneously reported as being closer to the system than the closer, duller, object. In a range finding system used to control robot machinery in an industrial setting, such errors may be intolerable for reasons of safety to nearby human operators. If such a system is used to identify and recognize different target objects, an object might be misidentified. Simply stated, two-dimensional intensity-based systems are very prone to measurement error.

[0005] The present invention may be used in a wide range of applications including, but not limited to, range finding systems. It may be useful at this juncture to briefly review such systems.

[0006] U.S. Patent No. 6,323,942 to Bamji et al. (Nov. 2001) entitled "CMOS-Compatible Three-Dimensional Image Sensor IC" describes a three-dimensional range finding system that can determine range distance without reliance upon luminosity-based data, the entire content of which patent is incorporated herein by this reference. As disclosed in the '942 patent, such a system generates a depth map that contains the distance  $Z$  from each pixel in a CMOS-compatible sensor array to a corresponding location on a target object. Applicants refer to and incorporate by reference the '942 patent as background material. U.S. patent no. 6,580,496 to Bamji et al. (June 2003) entitled "Systems for CMOS-Compatible Three-Dimensional Image Sensing Using Quantum Efficiency Modulation" describes the use of quantum modulation techniques and differential detectors suitable for a three-dimensional range finding system, the entire content of which patent is incorporated herein by this reference. In the '496 patent the quantum efficiency of the substrate upon which differential CMOS sensors were

fabricated was modulated synchronously with optical energy emitted from an energy source. Applicants refer to and incorporate by reference the '496 patent as background material.

[0007] Fig. 1 is a block diagram of a three-dimensional range finding system 10 as exemplified by the '942 patent or the '496 patent. Such systems determine distance Z between the system and locations on target object 20. System 10 may be fabricated upon a single IC 30, requires no moving parts, and relatively few off-chip components, primarily a source of optical energy 40, e.g., a light emitting diode (LED) or laser source, and associated optics 50. If desired, laser source 40 might be bonded onto the common substrate upon which IC 30 is fabricated.

[0008] System 10 includes an array 60 of pixel detectors 70, each of which has dedicated circuitry 80 for processing detection charge output by the associated detector. (As used herein, the terms "detector" and "pixel" and "pixel detector" may be used interchangeably.) Array 60 might include 100x100 pixels 70, and 100x100 associated detector processing circuits 80. One will appreciate that other configurations may be used. IC 30 preferably also includes a microprocessor or microcontroller unit 90, RAM and ROM memory, collectively 100, a high-speed distributable clock 110, and various computing and input/output (I/O) circuitry 120. System 10 preferably further includes a lens 130 to focus light reflected from target object 20 upon pixels 70 in array 60. As noted in the above-mentioned patents, controller unit 90 may carryout distance-to-object and object velocity calculations and can output such calculations as DATA, for use by a companion device, if desired. As seen in Fig. 1, substantially all of system 10 may be fabricated upon CMOS IC 30, which enables shorter signal paths, and reduced processing and delay times. Also shown in Fig. 1 is ambient light that is present in the environment in which system 10 and target object 20 are found. As described

herein, high levels of ambient light relative to levels of light from energy source 40 can be detrimental to reliable operation of system 10.

[0009] In brief, microprocessor 90 can calculate the roundtrip time for optical energy from source 40 to travel to target object 20 and be reflected back to a pixel 70 within array 60. This time-of-flight (TOF) is given by the following relationship:

$$\text{eq. (1): } Z = C \cdot t/2$$

where C is velocity of light.

[0010] Thus, without reliance upon luminosity information, system 10 can calculate that  $Z_1 = C \cdot t_1/2$ ,  $Z_2 = C \cdot t_2/2$ ,  $Z_3 = C \cdot t_3/2$ , and so on. The correct Z distances are obtained, even if more distant regions of target object 20 happen to be more reflective than nearer regions of the target object.

[0011] The ability of system 10 to determine proper TOF distances Z can be impacted when the magnitude of ambient light is large relative to the magnitude of reflected light from source 40. What occurs is that the various pixels 70 respond to incoming optical energy that represents the real signal to be measured (e.g., active energy originating from source 40 and reflected by target object 20), and also respond to ambient light. The depth resolution of each pixel, i.e., the accuracy of the distance measurement, is determined by the system signal-to-noise ratio (SNR). Even if ambient light could be measured and subtracted from the total signal, its noise component (e.g., shot noise) would still degrade system performance. Further, the presence of ambient light can have even more severe consequences by causing the pixel detector to saturate.

[0012] In a so-called differential pixel detector, the active optical energy contributes to both a differential mode signal and a common mode signal,

while ambient light only contributes to the common mode signal. While differential pixel detectors can exhibit higher SNR than single-ended pixel detectors, the presence of strong ambient light, sunlight perhaps, can degrade the performance of differential pixel detectors, as will now be described. As used herein, the term “differential detector” refers to a detector that responds to two input parameters. For example in the '496 patent, the differential detectors responded to amplitude of incoming optical energy and to phase of such energy relative to energy output by emitter 40; see Fig. 1 herein. Typically the singular term “pixel” will refer to a pair of differential photodetectors, for example first and second photodiode detectors  $D_A$  and  $D_B$ .

[0013] Incoming optical energy falling upon a pixel detector 70 generates an extremely small amount of photocurrent (or photocharge), typically on the order of picoamps ( $10^{-12}$  amps). Such detection current signals are too small in magnitude to be measured directly. It is known in the art to provide pixel detectors that operate in a direct integration mode by which optical energy induced photocurrent is integrated on a capacitor and the final capacitor charge or voltage is readout at the end of an integration interval. A capacitor  $C_x$  has finite maximum charge capacity  $Q_{max}$  defined by:

$$eq. (2): \quad Q_{max} = C_x \cdot V_{swing}$$

where  $C_x$  is the total capacitance and  $V_{swing}$  is the maximum voltage swing across the capacitor. A pixel detector is said to be in saturation when the total charge integrated on the capacitor exceeds the maximum charge capacity, in which case no useful information can be readout from that pixel.

[0014] A differential pixel detector (e.g., detectors 70 in Fig. 1) may be represented as shown generically in Fig. 2A, in which modulation circuitry has been omitted for simplicity. Each pixel 70 has a differential structure with two perhaps identical reset and readout circuit components denoted A and B. Components A and B may be considered as part of the pixel 70 or as part of

the pixel's associated circuitry 80. For ease of depictions, the photodetector pair comprising each differential pixel 70 is shown as photodiodes  $D_A$  and  $D_B$ , but other detector structures could be used instead, for example photogate structures. Capacitors  $C_A$  and  $C_B$  are shown in parallel with diodes  $D_A$  and  $D_B$  and represent detector parasitic capacitance and/or dedicated fixed value capacitors.

[0015] Referring briefly to Fig. 1, within system 10 microprocessor 90 causes optical energy source 40 to emit pulses of light that are directed by lens 50 toward target object 20. Some of this optical energy will be reflected back towards system 10 and will be focused by lens 130 onto pixels 70 within array 60. Incoming photon energy falling upon a detector 70 will cause photodetector pair  $D_A$  and  $D_B$  to generate a small amount of detection signal current that can be directly integrated by capacitors  $C_A$  and  $C_B$ . Before the start of integration, microprocessor 90 will cause photodetectors  $D_A$  and  $D_B$  and their respective capacitors  $C_A$  and  $C_B$  to be reset to a reference voltage  $V_{ref}$ . For the components shown in Fig. 2A, reset is caused by raising a reset signal  $\Phi_{reset}$  (see Fig. 2B). During the integration time, photocurrent generated by detectors  $D_A$  and  $D_B$  respectively discharge associated capacitors  $C_A$ ,  $C_B$ , as shown in Fig. 2B. During the integration time, the voltage seen at nodes  $S_A$ ,  $S_B$  will decrease as a function of the photocurrent generated by the associated photodiode  $D_A$ ,  $D_B$ . The magnitude of the photodiode-generated photocurrent will be a function of the amount of light energy received by the respective pixel 70 in array 60 in that the amount of light received by the pixel determines the final voltage on nodes  $S_A$  and  $S_B$ .

[0016] Readout circuitry is provided for circuit A and B, comprising transistors  $T_{follower}$  and  $T_{read}$ . At the end of the integration time, which will be a function of the repetition rate of the optical pulses emitted from optical energy source 40, microprocessor 90 causes a readout signal  $\Phi_{read}$  to go high. This enables the voltages on nodes  $S_A$  and  $S_B$  to be read-out of array 60, e.g., through a bitline.

In the exemplary configuration of Fig. 2A, if the voltage on node  $S_A$  or  $S_B$  drops below a certain level denoted here as saturation voltage  $V_{sat}$ , the readout circuit cannot perform the reading operation properly. Therefore the dynamic range of such known differential pixel configuration shown in Fig. 2A is  $(V_{ref} - V_{sat})$ , as depicted in Fig. 2B. While the waveforms in Fig. 2B depict a diminishing potential at nodes  $S_A$ ,  $S_B$  as a function of photocurrent, one could instead configure the detector circuitry to charge rather than discharge a reference node potential.

[0017] But in addition to generating photocurrent in response to optical energy or active light (from emitter 40) reflected by target object 20, pixel 70 will also generate photocurrent in response to ambient light that is also integrated by capacitors  $C_A$ ,  $C_B$ , thus affecting the potential at nodes  $S_A$ ,  $S_B$ . Fig. 2B depicts two examples, showing the effect of relatively low magnitude ambient light, and relatively high magnitude of ambient light. In range finding applications, the difference  $(A_{final} - B_{final})$  generally contains range information, and common mode is of lesser importance. As shown in Fig. 2B, relatively weak ambient light does not cause the pixel to saturate, and at the end of integration time, the final voltages read-out from the pixel are above  $V_{sat}$ . But relatively strong ambient light discharges the associated capacitor potential rapidly, which saturates the pixel. Due to the saturation condition, the pixel does not output any useful result in that the differential voltage, which contained range information, is now zero. Thus, a very real problem with prior differential pixel detectors is that the dynamic range of the pixel is not sufficient to handle strong ambient light.

[0018] Thus there is a need for a method and topology by which the dynamic range of a differential pixel detector can be enhanced such that degradation from ambient light is substantially reduced. Even in the presence of strong ambient light that might otherwise saturate the pixel, the differential response of the pixel should still be available. Further, such method and topology

should be implementable using CMOS such that the differential sensor array can still be fabricated on a common IC with associated range finding system.

[0019] Embodiments of the present invention provide such methods and circuit topologies.

## **SUMMARY OF THE INVENTION**

[0020] Effective differential dynamic range in a differential pixel detector is increased by avoiding saturation effects due to common mode contribution in optical energy to be detected. Photocurrent generated by each photodetector pair is directly integrated by an associated capacitor over an integration time  $T$ . The resultant capacitor voltage is proportional to detected optical energy including ambient light. Within time  $T$ , before either integrated capacitor voltage reaches  $V_{\text{sat}}$  for the photodetector, at least one of the capacitors is reset to a voltage such that the desired differential detector signal is still determinable.

[0021] In one embodiment, at start of integration time  $T$ , the voltage across each capacitor is preset to a fixed  $V_{\text{ref}}$  voltage. During integration time  $T$  whenever the integrated capacitor voltage of either capacitor reaches  $V_{\text{sat}}$ , that capacitor is reset to  $V_{\text{ref}}$ . After reset, capacitor voltages are again allowed to change as a function of photocurrent, and will be reset to  $V_{\text{ref}}$  whenever and as soon as either capacitor voltage reaches  $V_{\text{sat}}$ . A count of total resets for each capacitor is maintained, and the amount of light falling upon each detector is a function of its final voltage at end of integration and the number of resets occurring during integration. In another embodiment, the common mode component of the integrated capacitor voltages is reset periodically to prevent either photodiode detector from saturating. However the differential component of the integrated capacitor voltages is preserved. The result is to extend effective differential dynamic range of the differential sensor in the presence of ambient light by avoiding the effects of saturation. Embodiments



of the present invention can extend differential dynamic range of the differential sensor despite mismatching in the components implementing the differential pixel detector.

[0022] Other features and advantages of the invention will appear from the following description in which the preferred embodiments have been set forth in detail, in conjunction with the accompanying drawings.

### **BRIEF DESCRIPTION OF THE DRAWINGS**

[0023] FIG. 1 depicts a three-dimension TOF system using conventional pixel detectors as exemplified by U.S. Patent No. 6,323,942 and U.S. Patent No. 6,580,496;

[0024] FIG. 2A depicts a conventional differential pixel detector;

[0025] FIG. 2B depicts waveforms present in the detector of Fig. 2A showing the saturation effects of high ambient light;

[0026] FIG. 3A depicts one-half of a self-resetting differential pixel detector according to an embodiment of the present invention;

[0027] FIG. 3B depicts waveforms present in the detector of Fig. 3A, according to an embodiment of the present invention;

[0028] FIG. 3C depicts one-half of a self-resetting differential pixel detector implemented with an analog counter, according to an embodiment of the present invention;

[0029] FIG. 4A depicts one-half of a self-resetting differential pixel detector using an analog counter with reset, according to an embodiment of the present invention;

[0030] FIG. 4B depicts waveforms for a differential time to saturation counter as shown in Fig. 4A, according to an embodiment of the present invention;

[0031] FIG. 5A depicts a differential pixel detector using a controlled charge pump, according to an embodiment of the present invention;

[0032] FIG. 5B depicts waveforms present in the detector of Fig. 5A, according to an embodiment of the present invention;

[0033] FIG. 6A depicts a common mode resettable differential pixel detector, according to an embodiment of the present invention;

[0034] FIG. 6B depicts control waveforms present in the detector of Fig. 6A, according to an embodiment of the present invention;

[0035] FIG. 6C depicts waveforms present in the detector of Fig. 6A over a two reset sequence, according to an embodiment of the present invention;

[0036] FIG. 6D depicts another configuration of a common mode resettable differential pixel detector, according to an embodiment of the present invention;

[0037] FIG. 6E depicts yet another configuration of a common mode resettable differential pixel detector, according to an embodiment of the present invention;

[0038] FIG. 7A depicts a common mode resettable differential pixel detector using charge integration, according to an embodiment of the present invention;

[0039] FIG. 7B depicts control waveforms for the embodiment of Fig. 7A, according to the present invention;

[0040] FIG. 8A depicts a common mode resettable differential pixel detector with component mismatch cancellation using charge integration, according to an embodiment of the present invention;

[0041] FIG. 8B depicts waveforms associated with the configuration of Fig. 8A, according to an embodiment of the present invention;

[0042] FIG. 9A depicts a resettable differential pixel detector implemented with VCCS/CCCS current mirror, and an external control signal, according to an embodiment of the present invention;

[0043] FIG. 9B depicts a resettable differential pixel detector implemented with VCCS/CCCS current mirror, and a pulsed reference input signal, according to an embodiment of the present invention;

[0044] FIG. 9C depicts waveforms found in a current-source implemented differential pixel detector over a two reset sequence, according to an embodiment of the present invention;

[0045] FIG. 9D and FIG. 9E depicts two implementations of a CCCS current mirror for use in a differential pixel detector, according to an embodiment of the present invention;

[0046] FIG. 10A depicts a configuration for resetting common mode using a shunt capacitor, useable with a resettable differential pixel detector according to an embodiment of the present invention;

[0047] FIG. 10C depicts control waveforms found in the configuration of Fig. 10A, according to an embodiment of the present invention; and

[0048] FIG. 11 depicts a range finding type system using differential pixel detectors, according to the present invention.

## DETAILED DESCRIPTION OF THE INVENTION

[0049] Reference will now be made in detail to the preferred embodiments of the invention, examples of which are illustrated in the accompanying drawings. While the invention will be described in conjunction with the preferred embodiments, it will be understood that they are not intended to limit the invention to those embodiments. On the contrary, the invention is intended to cover alternatives, modifications and equivalents, which may be included within the spirit and scope of the invention as defined by the appended claims.

[0050] Fig. 3A depicts one-half of differential pixel detector 70', where it is understood that system 10 in Fig. 1 might now employ an array 60 of rows and columns of differential pixel detectors 70' in lieu of prior pixel detectors 70. In Fig. 3A, only one of the two pixels is shown for ease of illustration, namely photodetector  $D_A$  (denoted PD  $D_A$ ). Associated with each photodetector in the pixel is a capacitor,  $C_A$  being associated with  $D_A$ , where  $C_A$  can be the capacitance inherent with  $D_A$ , and/or a discrete capacitor. In a conventional configuration, in the presence of a signal, typically ambient light, the voltage across  $C_A$  would decrease until a saturation voltage  $V_{sat}$  was attained, at which point an output signal from  $D_A$  would be meaningless.

[0051] But as shown by the waveforms in Fig. 3B, the voltage at node  $S_A$ , e.g., the voltage across  $C_A$  and across  $D_A$ , is prevented from exceeding  $V_{sat}$  by resetting the node voltage to a fixed reference  $V_{ref}$  whenever  $V_{sat}$  is attained. Each differential pixel detector 70' includes two photodiodes and two capacitors, and each capacitor-photodiode node is independently reset to  $V_{ref}$ , as soon as the voltage across either capacitor reaches  $V_{sat}$ .

[0052] In Fig. 3A, a comparator 140 compares the voltage signal from photodiode  $D_A$  present at node  $S_A$  to  $V_{ref}$ . As soon as the  $S_A$  potential reaches  $V_{ref}$ , comparator 140 changes state, going from low-to-high for the

configuration shown. Thus when  $V_{S_A} > V_{sat}$ , the output from comparator 140 turns-on a reset transistor  $T_{reset}$  coupled between node  $S_A$  and  $V_{ref}$ . The potential  $V_{S_A}$  at node  $S_A$  is reset by being pulled from  $V_{sat}$  to  $V_{ref}$ . The desired result is that overall dynamic range of pixel detector 70' is increased.

[0053] Returning to Fig. 3A and 3B, the output from comparator 140 (node P) is also input to a counter 150 that essentially will count the number of resets that occur for the detector. It is understood that as Fig. 3A depicts half of a differential pixel detector, there will be two comparators, two counters, and two sets of switching transistors for each differential pixel detector 70'. The photodiode signal at node  $S_A$  is coupled via a high input impedance voltage follower transistor  $T_{follower}$ , whose output is read via a bitline when a  $\Phi_{readA}$  signal goes high (for the configuration shown). An additional row selection transistor  $T_{readD}$  is coupled between the output from counter 150 and the bitline signal, and is turned on when a  $\Phi_{readD}$  signal goes high (for the configuration shown). Note that a feedback path exists between the comparator output and the gate for reset transistor  $T_{reset}$ . Those skilled in the art will appreciate that means other than the above described solid state switches, comparators, counters, etc., may be used to implement similar embodiments of the present invention.

[0054] Referring briefly to Fig. 1, optical energy source 40 typically outputs a pulse train of optical energy, which energy may be modulated, for example according to the '496 patent. The pulse train will have a period between adjacent output pulses. Within differential detector 70', the maximum period of integration is made less than the period between adjacent pulses of optical energy emitted by source 40. Referring back to Figs. 3A and 3B, during integration in the presence of strong ambient light, sunlight perhaps, the voltage at node  $S_A$  across  $C_A$  continues to decrease in magnitude until  $V_{sat}$  is reached. At that moment, comparator 140 changes states, emitting a short output pulse that is present at node P. This pulse turns-on reset transistor  $T_{reset}$  for a short

time, causing  $C_A$  to be again reset to voltage  $V_{ref}$ . Such reset is self-triggering, and can occur multiple times during the integration interval. The total number of such resets is recorded by counter 150, there being one counter for each of the two photodiode detectors in a differential pixel detector 70'.

[0055] At the end of the integration time, the counter value ( $n$ ) and the final voltage  $V_{final}$  on capacitor  $C_A$  are read-out separately by turning-on  $T_{readD}$  and  $T_{readA}$ , respectively. Fig. 3A is conceptual in that while counter 150 is shown being read-out as though its counter  $n$  were an analog value, in practice the digital counter will be read-out with a bus. The signal waveforms for node  $S_A$  and the comparator output at node P are shown in Fig. 3B. Note that the effective voltage swing on node  $S_A$  is  $V_{swing} = n(V_{ref} - V_{sat}) + V_{final}$ , which is  $n$  times larger than the maximum voltage swing ( $V_{ref} - V_{sat}$ ) of known differential sensors. Thus using the self-resetting configuration of Fig. 3A, capacity is extended by  $n$  times, where  $n$  is the number of self-resets occurring during integration. The resultant extended maximum charge capacity for the photodiode enables the pixel sensor to detect differential mode signals even in the presence of very strong ambient light.

[0056] While Fig. 3A has been described with respect to use of a counter 150 that operates digitally, the role of counter 150 can instead be implemented in analog fashion. Fig. 3C depicts such an implementation, in which an analog charge pump produces an analog voltage value proportional to  $n$ . Such an analog circuit can be implemented using small area on an IC, e.g., IC 30 in Fig. 1, where conventional detectors 70 are replaced by detectors 70' according to the present invention.

[0057] In Fig. 3C, a current source changes voltage across a capacitor  $C_r$ , where each time a reset pulse (of fixed duration) is generated by comparator 140, the current source is turned on. Thus for each comparator reset pulse, a

fixed amount of charge is injected into capacitor  $C_r$ , altering the voltage across the capacitor by  $\Delta V_r$ . At the end of the integration time, the voltage on capacitor  $C_r$  changes by an amount equal to  $\Delta V_r$  times the number of reset pulses  $n$  that occurred during integration. It is possible to determine  $n$  by  $n = (V_{ref} - V_r)/\Delta V_r$ . Note that capacitor  $C_r$  is also initialized to  $V_{ref}$  when the photodetector is initialized. If desired, an initial voltage other than  $V_{ref}$  could be used for capacitor  $C_r$ .

[0058] In Fig. 3C, photodetector  $D_A$  can be reset by using the non-inverting input of comparator 140, which input normally is set to  $V_{sat}$ . But this non-inverting input can be used to perform an initial (frame) reset before integration. For example, during the initial reset period this input can be switched to  $V_{DD}$ , which will cause the comparator to output a pulse at node P that resets  $T_{reset}$  and thus resets photodetector  $D_A$  and its associated capacitor  $C_A$ . Thereafter the non-inverting node of comparator 140 can be returned to  $V_{sat}$  to remain at that potential until the next (frame) reset. By judiciously making voltage  $V_{sat}$  low, all photodetectors are simultaneously reset, thus removing the need for a separate reset signal.

[0059] Turning now to Figs. 4A and 4B, an embodiment of a differential comparator is described in which a differential time to saturation counter is employed. In the block diagram of Fig. 4A a single detector PD  $D_A$  is shown, although it is understood that a complete differential pixel detector 70' will comprise two detector diodes (or the like), two comparators, a counter, and associated reset and read-out transistors. In Fig. 4A, while counter 150' is shown implemented with analog components, a counter could instead be implemented to function digitally.

[0060] At start of integration, counter 150' starts counting to measure the time since the last reset to  $V_{ref}$ . In the following discussion it will be assumed that the magnitude of incoming ambient light does not change substantially during

the integration time. Two scenarios will be considered: ambient light is strong, and ambient light is not very strong.

[0061] If the ambient light is strong, each photodetector  $D_A$  and  $D_B$  ( $D_B$  not shown) will reach  $V_{sat}$  multiple times during one integration period. In this case, every time either photodetector reaches  $V_{sat}$ , the photodetectors and counter 150' are simultaneously reset. At the end of the integration period, each photodetector will be at a determinable voltage level, which level will likely be different for each detector. Further, at the end of the integration period, the counter will have stored the time ( $\Delta t_f$ ) since the last reset required for the photodetectors to attain these final voltage levels. Since each photodetector end-of-integration voltage level is known, as is the time  $\Delta t_f$ , the slope of the voltage curves for each photodetector and the number of resets that should have occurred during integration can be determined; see Fig. 4B. Note at the right-hand side of Fig. 4B that the final photodiode voltages are  $(V_{ref} - \Delta V_{af})$  and  $(V_{ref} - \Delta V_{bf})$  for photodiodes  $D_A$  and  $D_B$  respectively. Subtracting these magnitudes from  $V_{ref}$  yields  $\Delta V_{af}$  and  $\Delta V_{bf}$ . The total swing can be calculated as follows:

$$eq. (3): \quad V_{swing-a} = \Delta V_{af} \cdot T / \Delta t_f$$

$$eq. (4): \quad V_{swing-b} = \Delta V_{bf} \cdot T / \Delta t_f$$

where  $T$  is the total integration time, which is known.

[0062] If the ambient light is not strong, at the end of the integration time  $T$ , the counter value will be equal to the integration time, and the voltages across the photodiodes  $D_A$  and  $D_B$  will represent all that the photocharge each pixel could collect during the whole integration time. In this case, no further calculation is needed to determine the total voltages, since it follows from  $T = \Delta t_f$  that:

$$eq. (5): \quad V_{swing-a} = \Delta V_{af}$$



eq. (6):  $V_{swing-b} = \Delta V_{bf}$

[0063] Once the relevant times and photodiode voltages are read-out, an external computation unit, perhaps microprocessor 90 in system 10 (see Fig. 1) or pure logic circuitry can calculate to provide the differential signal.

[0064] As noted, in Fig. 4A an analog equivalent of a digital resettable counter 150' is used, in which a charge pump can be used to measure  $\Delta t_f$ . A charge pump capacitor  $C_r$  is reset by transistor  $T_{Creset}$  each time photodiode voltage reaches  $V_{sat}$ . Thus at the end of time  $T$ , the voltage on  $C_r$  is proportional to the time from the last reset to the end of integration. Assuming the constant current supplied to  $C_r$  is  $I_r$ , then the final voltage on  $C_r$  will be  $V_r = V_{ref} - I_r \cdot \Delta t_f / C_r$  and  $\Delta t_f$  can be determined as  $\Delta t_f = (V_{ref} - V_r) \cdot C_r / I_r$ . In the above descriptions, two independent counters are present. However since only the counter causing the most recent reset is of use, both counters can be combined into a single counter. This single counter and the reset for both halves of the pixel detector could be controlled by the logical OR of both comparators.

[0065] As noted, capacitor  $C_r$  is initialized at the beginning of integration along with the photodetector. As with the self-reset method, the non-inverting input of comparator 140 may be switched to  $V_{DD}$  (rather than to  $V_{sat}$  during integration) to reset pixel 70' (e.g., both photodetectors and  $C_r$ ). By judiciously making voltage  $V_{sat}$  low, all photodiodes are simultaneously reset, thus removing the need for a separate reset signal.

[0066] Turning now to Figs. 5A and 5B an embodiment of the present invention is shown in differential pixel detector 70' includes a voltage controlled charge pump 160 to record voltage difference between the two differential photodetectors  $D_A$  and  $D_B$  before they are saturated by high common mode signal. Once the photodetector voltage difference has been recorded on a third capacitor  $C_r$ , photodetectors  $D_A$  and  $D_B$  and their

associated capacitors ( $C_A$ ,  $C_B$ ) can be reset by the relevant reset transistors, and integration starts again.

[0067] In Fig. 5A, charge pump 160 includes two voltage controlled current sources  $I_{s1}$ ,  $I_{s2}$  and a capacitor  $C_r$ . Although the voltage difference between photodetectors  $D_A$  and  $D_B$  may be monitored continuously by differential amplifier 170, charge pump 160 is only turned-on for a fixed period of time. In this fashion, charge accumulated on capacitor  $C_r$  during each sample is proportional to the voltage difference. After each sample, the differential photodetector is reset and a new integration cycle starts. The sampling frequency preferably depends upon incoming light intensity, e.g., optical energy falling upon photodetectors  $D_A$  and  $D_B$ , which intensity can be estimated. The final charge on  $C_r$  is the summation of the samples and is proportional to the total voltage difference between the differential photodetectors. Fig. 5B depicts control signal and voltage waveforms at various nodes in the configuration of Fig. 5A.

[0068] At the end of integration, three voltage values are read-out from pixel 70', namely  $V_a$  (voltage across  $D_A$ ),  $V_b$  (voltage across  $D_B$ ), and  $V_r$  (voltage across capacitor  $C_r$ ). Given these quantities, one can calculate the resulting differential voltage  $V_{\text{swing-a}} - V_{\text{swing-b}}$  as follows. Looking at Fig. 5B, it is seen that  $\Delta V_{af} = V_{\text{ref}} - V_a$  and that  $\Delta V_{bf} = V_{\text{ref}} - V_b$ . The differential voltage is then given by  $V_{\text{swing-a}} - V_{\text{swing-b}} = \Delta V_{af} - \Delta V_{bf} + f(V_r)$ , where  $f(V_r)$  is a linear function of  $V_r$ .

[0069] This linear function  $f(V_r)$  is obtained by writing  $V_r$  as  $V_r = V_{\text{ref}} + n \cdot k \cdot (V_a - V_b)$ . As noted,  $V_{\text{ref}}$  is the initial voltage for capacitor  $C_r$  (e.g., the reset voltage for photodetectors  $D_A$ ,  $D_B$ ),  $n$  is the number of sample/reset cycles, and  $k$  is a constant determined from the circuit of Fig. 4A, and represents how much voltage change occurs on  $C_r$  for given a unit voltage change in  $(V_a - V_b)$ . The amount contributing to  $V_{\text{swing-a}} - V_{\text{swing-b}}$  is  $n \cdot (V_a - V_b)$ , which is equal to  $n \cdot$

$(V_a - V_b) = (V_r - V_{ref})/k = f(V_r)$ . In summary the final differential voltage is calculated from known quantities, according to  $V_{swing-a} - V_{swing-b} = V_b - V_a + (V_r - V_{ref})/k$ . Common mode voltage can also be estimated from  $\Delta V_{af}$  and  $\Delta V_{bf}$  since the time between the last reset and the end of integration is known.

[0070] It is possible to automatically generate the  $\Delta_{sample}$  or  $\Delta_{reset}$  signals within each pixel 70', by providing some additional circuitry. One can use two comparators to compare  $S_A$ ,  $S_B$  node potentials with  $V_{sat}$ , and the logical OR can be taken of the comparator outputs to yield the  $\Delta_{sample}$  signal. Thus as soon as either photodiode potential reaches  $V_{sat}$ ,  $\Delta_{sample}$  goes high. If desired,  $\Delta_{reset}$  can be a delayed version of  $\Delta_{sample}$ . Such a self-resetting configuration would use two comparators, an OR gate, and a delay element that could be a simple RC delay.

[0071] Turning now to Fig. 6A, an embodiment of a differential pixel detector 70' is shown in which during reset operation capacitors acquire exactly the same charge in each half of the configuration. By adding exactly the same charge to each half of the configuration, common mode contribution is essentially removed and differential mode contribution is preserved. Such an approach offers several advantages. For example, extra resets do not affect the system operation, and the pixel detector may be reset even if it is not discharged. Further, capacitor or component mismatch has substantially no effect on the accuracy of the reset. In addition, it can be shown that common mode reset generates no  $KT/C$  noise in the differential domain. The only resulting  $KT/C$  contribution appears in common mode where it is unimportant.

[0072] For ease of illustration, Fig. 6A does not depict  $Q_A$ , which is the sum of the charge on the top plate of capacitors  $C_A$  and  $C_{DA}$ , or  $Q_B$ , which is the sum of the charge on the top plate of capacitors  $C_B$  and  $C_{DB}$ . In operation, the configuration of Fig. 6A preserves the differential quantity  $Q_A - Q_B$  during the common mode reset operation, although the common mode quantity,  $(Q_A +$

$Q_B)/2$ , is changed at each reset. What occurs is that after a reset, the quantity  $(Q_A + Q_B)/2$  is moved closer to some constant  $Q_{\text{reset0}}$ . Thus in contrast to other reset approaches, additional resets have no adverse impact in Fig. 6A as they simply move the operating point for  $(Q_A + Q_B)/2$  even closer to  $Q_{\text{reset0}}$ .

[0073] In normal operation switching transistors  $T_{\text{swA}}$  and  $T_{\text{swB}}$  are open, while transistors  $T_{\text{vrefA}}$  and  $T_{\text{vrefB}}$ , and  $T_{\text{disA}}$  and  $T_{\text{disB}}$  are closed. Initially photodetector diodes  $D_A$  and  $D_B$  are reset to  $V_{\text{ref}}$  via transistors  $T_{\text{resetA}}$  and  $T_{\text{resetB}}$ , but during integration transistors  $T_{\text{resetA}}$  and  $T_{\text{resetB}}$  remain open. As optical energy impinges on photodiode  $D_A$  it discharges its parasitic capacitor  $C_{\text{DA}}$  as well as capacitor  $C_A$ , while photodiode  $D_B$  discharges its parasitic capacitor  $C_{\text{DB}}$  as well as its capacitor  $C_B$ . Initial reset is achieved through transistors  $T_{\text{resetA}}$  and  $T_{\text{resetB}}$ , which initialize the circuit at potential  $V_{\text{ref}}$ , although other potential levels may instead be used.

[0074] During common mode reset, signal  $\Phi_{\text{resetA}}$  remains low, while the other control signals operate as shown in Fig. 6B. During operation of pixel 70', the following steps take place:

[0075] (1) First, capacitors  $C_A$  and  $C_B$  are decoupled from associated photodiodes  $D_A$  and  $D_B$  by bringing the  $\Phi_{\text{dis}}$  signal low, which opens discharge transistors  $T_{\text{disA}}$  and  $T_{\text{disB}}$  going low. This operation does not change the differential charge quantity  $Q_A - Q_B$ , and no  $KT/C$  noise is introduced on  $Q_A - Q_B$ .

[0076] (2) Next, when control signal  $\Phi_{\text{norm}}$  goes low, the bottom plates of capacitors  $C_A$  and  $C_B$  are decoupled from  $V_{\text{ref}}$  by the opening of transistors  $T_{\text{refA}}$  and  $T_{\text{refB}}$ . The quantity  $Q_A - Q_B$  remains unaffected, even in terms of  $KT/C$ .

[0077] (3) When the control signal  $\Phi_{\text{switch}}$  goes high, capacitors  $C_A$  and  $C_B$  redistribute their charge. Let  $Q_{\text{CA}}$  be the charge on capacitor  $C_A$  and let  $Q_{\text{CB}}$  be the charge on capacitor  $C_B$ . If capacitors  $C_A$  and  $C_B$  are now shorted

together in parallel the total charge quantity  $Q_{CA} + Q_{CB}$  would be preserved. However since  $C_B$  is connected to  $C_A$  inverted, the quantity  $Q_{CA} - Q_{CB}$  is preserved during this operation. Since no switches are opened no  $KT/C$  arises from this step.

[0078] (4) When the control signal  $\Phi_{swA}$  goes low; a  $KT/C$  uncertainty appears in the charge redistribution, but this  $KT/C$  appears as common mode on the quantities  $Q_{CA}$  and  $Q_{CB}$ . Any charge taken from  $Q_{CA}$  shows up exactly on  $Q_{CB}$  but with a minus sign. Thus after switches  $T_{swA}$  and  $T_{swB}$  open,  $Q_{CA}' = Q_{CA} + \text{Noise}_{KTC}$ , and  $-Q_{CB}' = -Q_{CB}' - \text{Noise}_{KTC}$ . Thus there is no  $KT/C$  noise on  $Q_{CA}' - Q_{CB}' = Q_{CA} - Q_{CB} + (\text{Noise}_{KTC} - \text{Noise}_{KTC})$ :

[0079] (5) Next, when control signal  $\Phi_{norm}$  goes high again the differential charge  $Q_A - Q_B$  is unchanged.

[0080] (6) Finally, when control signal  $\Phi_{dis}$  goes high,  $Q_A - Q_B$  is unchanged.

[0081] If desired some of the above steps may be combined for simplicity. For example steps 5 and 6 may occur simultaneously or even out of sequence. Steps 1,2 and 5,6 clearly do not affect  $Q_A - Q_B$ , and it was demonstrated that steps 3 and 4 do not affect  $Q_{CA} - Q_{CB}$ . Thus, steps 1 through 6 do not affect  $Q_A - Q_B$ . In operation, the generation of the various control signals can be handled by microprocessor 90 in system 10 in Fig. 1, where it is understood that array will comprise differential pixels 70', according to the present invention.

[0082] Note that no assumption as to closeness of component matching was made in the above analysis, and the conclusions reached remain irrespective of the values of capacitors  $C_A$ ,  $C_B$ ,  $C_{DA}$ , and  $C_{DB}$ . Additionally the linearity of the capacitors does not affect performance, and the configuration shown in Fig. 6A will function with capacitors that are mismatched or even nonlinear.

[0083] Consider now the common mode voltage on photodiodes  $D_A$  and  $D_B$  after reset. Within reasonable bounds, the exact value of the common mode voltage is not critical. Although an analysis can be carried out for almost any capacitor values, for simplicity of explanation let it be assumed that  $C_A = C_B$  and  $C_{DA} = C_{DB}$ .

[0084] Since it is small, let  $KT/C$  reset noise be ignored. Thus after step 5 if  $V_{CA}$  (the voltage across capacitor  $C_A$ ) and if  $V_{CB}$  (the voltage across capacitor  $C_B$ ) have the relation  $V_{CA} = -V_{CB}$ , the voltage on the top plate of  $C_A$  is  $(V_{ref} + V_{CA})$  and the voltage on the top plate of  $C_B$  is  $(V_{ref} - V_{CA})$ .

[0085] As noted, charge difference  $Q_A - Q_B$  is preserved in the configuration of Fig. 6A. Assuming that  $C_A = C_A$  and  $C_{DA} = C_{DB}$  it can be shown that the voltage difference  $V_{DA} - V_{DB}$  on the photodiodes is also preserved, and that is voltage is  $V_{DA} - V_{DB} = 2V_{CA} = -2V_{CB}$ , after step 5. Thus following step 5,  $V_{DA}$  and  $V_{DB}$  must differ from the top plate voltages on capacitors  $C_A$  and  $C_B$  by only a constant  $K$ .

$$\text{eq. (7): } V_{DA} = V_{ref} + V_{CA} + K$$

$$\text{eq. (8): } V_{DB} = V_{ref} + V_{CB} + K = V_{ref} - V_{CA} + K$$

$$\text{eq. (9): } V_{DA} + V_{DB} = V_{ref} + V_{CA} + K + V_{ref} - V_{CA} + K = 2(V_{ref} + K)$$

[0086] After step 6 because of charge redistribution the new voltages are:

$$\text{eq. (10): } V_{DA}' = [C_{DA} \cdot V_{DA} + C_A \cdot (V_{ref} + V_{CA})] / (C_{DA} + C_A)$$

$$\text{eq. (11): } = [C_{DA} \cdot (V_{ref} + V_{CA} + K) + C_A \cdot (V_{ref} + V_{CA})] / (C_{DA} + C_A)$$

$$\text{eq. (12): } = [(V_{ref} + V_{CA}) + C_{DA} \cdot K / (C_{DA} + C_A)], \text{ and}$$

$$\text{eq. (13): } V_{DB}' = [C_{DB} \cdot V_{DB} + C_B \cdot (V_{ref} + V_{CB})] / (C_{DB} + C_B)$$

$$\text{eq. (14): } = [C_{DB} \cdot (V_{ref} + V_{CB} + K) + C_B \cdot (V_{ref} + V_{CB})] / (C_{DB} + C_B)$$

$$\text{eq. (15): } = [(V_{ref} + V_{CB}) + C_{DB} \cdot K / (C_{DB} + C_B)]$$

$$eq. (16): \quad = [(V_{ref} - V_{CA}) + C_{DA} \cdot K / (C_{DA} + C_A)]$$

Thus the sum  $V_{DA}' + V_{DB}'$  then becomes

$$eq. (17): \quad V_{DA}' + V_{DB}' = [(V_{ref} + V_{CA}) + C_{DA} \cdot K / (C_{DA} + C_A)] + [(V_{ref} - V_{CA}) + C_{DA} \cdot K / (C_{DA} + C_A)] = 2 \cdot [V_{ref} + K \cdot C_{DA} / (C_{DA} + C_A)]$$

Thus the sum  $V_{DA}' + V_{DB}'$  is advantageously always closer to  $2V_{ref}$  than to  $V_{DA} + V_{DB}$ . This demonstrates that with each reset in Fig. 6A, the common mode is brought closer to  $V_{ref}$  by  $K \cdot [1 - C_{DA} / (C_{DA} + C_A)] = K \cdot C_A / (C_{DA} + C_A)$ .

[0087] To recapitulate, for the embodiment of Fig 6A, reset operation has the desired effect of centering the common mode about  $V_{ref}$ . Relevant waveforms for Fig. 6A are shown in Fig. 6C. As a consequence, a reset can be applied without consideration of over-saturating or under-saturating the common mode for the pixel configuration. Thus in normal operation, reset can occur as often as desired without concern as to ill effects resulting from over or under saturation of the common mode.

[0088] Transistors  $T_{disA}$  and  $T_{disB}$  can be used as global shutters, thereby improving resilience to ambient light by stopping the effects of all light impinging on the differential pixel when the shutter is turned off. When  $T_{disA}$  and  $T_{disB}$  are off, capacitors  $C_a$  and  $C_b$  are decoupled from photodetectors  $PD_{DA}$  and  $PD_{DB}$  and therefore stop integrating the signal from  $PD_{DA}$  and  $PD_{DB}$ . If the output of the pixel is chosen to be top plate of capacitors  $C_A$  and  $C_B$  then the output of the pixel will be frozen after  $T_{disA}$  and  $T_{disB}$  are turned-off, thereby providing the function of a global shutter.

[0089] Fig. 6D depicts another embodiment of a capacitor common mode reset configuration for pixel 70', according to the present invention. Basic operation for the configuration of Fig. 6D is as described for the configuration of Fig. 6A. However, in Fig. 6D, initialization of voltages  $V_{DA}$  and  $V_{DB}$  across photodiodes  $D_A$ ,  $D_B$  respectively at the beginning of integration does not

involve transistors  $T_{\text{resetA}}$  and  $T_{\text{resetB}}$  as was the case for the configuration of Fig. 6A. Instead, in Fig. 6D, reset is achieved by simultaneously turning-on transistors  $T_{\text{disA}}$  and  $T_{\text{disB}}$  with high control signals  $\Phi_{\text{dis}}$ , turning-on transistors  $T_{\text{swA}}$  and  $T_{\text{swB}}$  with high control signal  $\Phi_{\text{sw}}$ , and by turning-off transistors  $T_{\text{VrefA}}$  and  $T_{\text{VrefB}}$  with low control signal  $\Phi_{\text{norm}}$ . This has the effect of resetting photodetectors  $\text{PDD}_A$  and  $\text{PDD}_B$  to  $V_{\text{ref}}$ . Note that transistors  $T_{\text{disA}}$  and  $T_{\text{disB}}$  may be used as global shutters in this configuration.

[0090] Fig. 6E depicts yet another embodiment for pixel 70', wherein discharge transistors  $T_{\text{disA}}$  and  $T_{\text{disB}}$  are eliminated. Indeed these discharge transistors could also be removed from the configurations of Fig. 6A and Fig. 6D. While these alternative configurations reduced common mode, unfortunately detector performance is diminished. This degradation results as each reset reduces some of the differential mode signal, and after a usually small number of resets, the differential signal is lost as a function of  $C_{\text{DA}}/C_A$  and  $C_{\text{DB}}/C_B$ . Such embodiments may still find use in applications that do not require high precision, or where the number of resets is low, or where  $C_{\text{DA}} \ll C_A$  and  $C_{\text{DB}} \ll C_B$ .

[0091] Turning now to Figs. 7A and 7B, a configuration and waveforms for a differential pixel detector 70' is shown in which a charge integrator is used for differential signal integration and common mode reset. Integration is carried out by integrator 180 and integration capacitor  $C_{\text{int}}$ . During an initial frame reset, transistors controlled by  $\Phi_{\text{reset}}$ ,  $\Phi_r$ , and  $\Phi_{\text{int}}$  signals are all turned-on, and the voltages on photodetectors  $D_A$  and  $D_B$  are reset to  $V_{\text{ref}}$ .

[0092] During integration, transistors controlled by signal  $\Phi_{\text{int}}$  are turned-on and transistors controlled by signals  $\Phi_r$ ,  $\Phi_{\text{reset}}$  are turned-off. Thus during integration, light induced photocurrent discharges photodiode parasitic capacitance  $C_{\text{DA}}$ ,  $C_{\text{DB}}$ , as well as capacitors  $C_A$  and  $C_B$ . As has been noted, the integrated signals contain both differential mode and common mode



components. Fig. 7B depicts various control voltage waveforms used in the embodiment of Fig. 7A.

[0093] Next, in a common mode reset phase, control signal  $\Phi_{\text{int}}$  goes low, causing transistors  $T_{\text{int}}$  to decouple  $C_A$  from  $C_{DA}$  and to decouple  $C_B$  from  $C_{DB}$ . Then control signal  $\Phi_r$  goes high, turning-on transistors  $T_r$  and charge in both  $C_A$  and  $C_B$  transfers to the integration capacitor  $C_{\text{int}}$ . Note that polarities of the charge transferred onto  $C_{\text{int}}$  are opposite due to the arrangement of the  $T_r$  switches.

[0094] The integrated charge on  $C_{\text{int}}$  after the common mode reset can be expressed in terms of charge on  $C_{DA}$ ,  $C_{DB}$  before the common mode reset as:

$$\text{eq. (18): } Q_{\text{int}} = Q_{C_{DA}} - Q_{C_{DB}}$$

[0095] Therefore the common mode signal is cancelled while the differential signal is preserved, which is the desired result.

[0096] Preferably common mode reset is performed multiple times and is interleaved with the integration during the whole frame integration. During integration, the integrating operational amplifier 180 may be turned off to save power. The total number of common mode reset performed will depend on the intensity of ambient light. The final signal readout is the accumulated charge (hence voltage) on  $C_{\text{int}}$ .

[0097] While the charge integrator in the embodiment of Fig. 7A used a single-ended operational amplifier 180, a fully differential operational amplifier could be used, among other types of integration configurations.

[0098] In the embodiment of Fig. 7A, each differential pixel (e.g., each  $D_A$  and  $D_B$  photodiode pair) has its own integrator, e.g., 180. In an alternative embodiment, one can implement only integration capacitor  $C_{\text{int}}$  within each

pixel, and share operational amplifier 180 as well as switches associated with connecting  $C_{int}$  to amplifier 180 among multiple pixels. This approach would require fewer transistors per pixel, allowing a higher fill factor to be achieved on the integrated circuit containing the detector system.

[0099] Turning now to Fig. 8A, an embodiment of a differential detector 170' is shown in which the common mode reset circuitry compensates for potential mismatch between components such as mismatched detector area between  $D_A$  and  $D_B$ , mismatched tolerance between capacitors  $C_A$  and  $C_B$ , as well as mismatched transistor sizes.

[0100] Fig. 8B depicts control waveforms found in an alternate embodiment of Fig. 8A. In this alternate embodiment, as shown in Fig. 8B, the phase of the optical energy waveform from emitter 40 (LIGHT) alternates between  $0^\circ$  and  $180^\circ$  with respect to the phase of a signal used to modulate the photodetectors. Thus, rather than use fixed charge transfer polarity as in the embodiment of Fig. 7B, polarity between  $D_A$  and  $D_B$  is switched synchronously in time with modulation of the light emitted from system 10 towards target object 20. The accumulated charge on integration capacitor  $C_{int}$  at the end of frame integration is expressed as:

$$\begin{aligned} eq. (19): \quad Q_{int} &= (Q_{A,0}^1 - Q_{B,0}^1) + (Q_{A,180}^1 - Q_{B,180}^1) + (Q_{A,0}^2 - Q_{B,0}^2) + (Q_{A,180}^2 - Q_{B,180}^2) + \dots \\ &= \sum_{i=1}^{n/2} (Q_{A,0}^i - Q_{B,0}^i) + \sum_{i=1}^{n/2} (Q_{A,180}^i - Q_{B,180}^i) \end{aligned}$$

where  $Q_{A,0}$  represents the charge collected by detector  $D_A$  with respect to  $0^\circ$  light phase,  $Q_{B,0}$  represents the charge collected by detector  $D_B$  with respect to  $0^\circ$  light phase,  $Q_{A,180}$  represents the charge collected by detector  $D_A$  with respect to  $180^\circ$  light phase, and  $Q_{B,180}$  represents the charge collected by detector  $D_B$  with respect to  $180^\circ$  light phase. As is apparent from the above equation, if the total number of common mode resets is  $n$ , then half of the final

differential charge is collected from detector  $D_A$  and half of the charge is collected from detector  $D_B$ . Another advantage of this embodiment is that  $KT/C$  noise associated with the transistor switches becomes common mode; therefore such noise is cancelled out from the final differential signal value.

[00101] Most of the above-described embodiments accumulate the  $D_A-D_B$  charge difference in a capacitor, and periodically reset  $D_A$  and  $D_B$  to  $V_{ref}$  to avoid saturation. Fig. 9A depicts an alternative approach in which potentials  $V_a$  and  $V_b$  are increased by a fixed amount  $\Delta V$  before these potentials drop below a certain level due to high-common mode light. This approach is somewhat analogous to the capacitor common mode reset embodiments that have been described. However the embodiment of Fig. 9A uses a separate circuit with an external current source 190.

[00102] In the embodiment of Fig. 9A, a periodic injection of a fixed amount of charge into detectors  $D_A$  and  $D_B$  occurs. The result is that while the differential ( $D_A-D_B$ ) charge does not change, the common mode of  $D_A$  and  $D_B$  is refreshed (i.e., decreased) to prevent photodetector saturation. An external current source 190 is required, which current source may be a reference Voltage Controlled Current Source (VCCS) or perhaps a reference Constant Current Controlled Current source (CCCS), in which case the current source becomes a current mirror.

[00103] The embodiment of Fig. 9A and the embodiment of Fig. 9B demonstrate two approaches to periodically refreshing charge into detectors  $D_A$  and  $D_B$ . In Fig. 9A, current source 190 is always on, but switches  $T_{sw}$  responsive to an external signal  $\Phi_{XC}$  are used to couple the constant current output by source 190 to nodes  $S_A$  and  $S_B$ . During integration  $\Phi_{XC}$  is periodically turned-on for a brief period of time to charge-up nodes  $S_A$  and  $S_B$ , hundreds of nanoseconds perhaps.

[00104] In the embodiment of Fig. 9B, switches  $T_{sw}$  are eliminated and instead the input current or voltage to current source 190 is itself pulsed. In essence rather than import a signal  $\Phi_{XC}$ ,  $\Phi_{XC}$  pulses are imported into current source 190 and result in current pulses of constant amplitude as shown.

[00105] Fig. 9C depicts waveforms for the configurations of Figs. 9A and 9B. Note that advantageously the final differential voltage is simply  $(V_A - V_B)$  and that no other computation need be done. The rate at which  $\Phi_{XC}$  or the reference input to current count 190 will depend upon the common mode ambient light. A higher rate would be called for in the presence of very strong ambient light to keep source nodes  $S_A$  and  $S_B$  from saturating.

[00106] As noted, current source 190 may be controlled using a voltage reference or a current reference. If a voltage reference is used, the voltage can be  $V_{DD}$  or  $V_{ref}$ , in which case only the  $\Phi_{XC}$  signal would be needed to perform common-mode removal. For CCCS (or current mirrors) a variety of circuit configurations and structures are available, two of which are shown in Figs. 9D and 9E. While the configuration of Fig. 9D has fewer components, its current output may suffer from nonlinearity caused by transistor channel length modulation. The configuration of Fig. 9E provides a cascoded current mirror that is insensitive to voltage at the current output nodes. The choice of current source configuration involves a tradeoff between circuit complexity and accuracy.

[00107] An important concern in implementing current mirrors is matching, in this case between output currents A and B. To minimize matching errors, transistors with large values of width and length should be used and should be carefully laid out. For example the orientation of transistors should be the same for currents A and B.

[00108] Fig. 10A depicts a shunt capacitor embodiment of the present invention to periodically inject a certain amount of charge into photodetector  $D_A$  and  $D_B$  to compensate for the common mode. Fig. 10A depicts one-half of such a circuit, while Fig. 10B depicts control signal waveforms. A, preferably, very small capacitor  $C_{\text{charge}}$  is initially charged-up to a relatively high voltage. When charge signal  $\Phi_{\text{charge}}$  goes low and reset signal  $\Phi_{\text{reset}}$  goes high,  $C_{\text{charge}}$  and  $C_A$  are connected, and most of the charge will be transferred to  $C_A$  since its capacitance is much higher than  $C_{\text{charge}}$ . Since the same amount of charge is added into both halves of the configuration, the common mode signal is reset while the differential mode signal is preserved.

[00109] Fig. 11 is a block diagram of a range finding system 10 using differential pixel detectors 70' according to any of the embodiments described herein. In Fig. 11, target object 20' is an image of a input device, for example an image of a computer keyboard. The image may be printed on a piece of paper or may in fact be optically projected from within system 10. However presented, target object 20' is visible to a user who can type upon the image as though it were a real keyboard. System 10 can measure in three-dimensions the location of whichever virtual keys are typed upon by the user, and in what time order, e.g., did the user type "am" or "ma". This information, which can be obtained even in strong ambient light, can then be passed to a companion device 200, perhaps a cellular telephone, a PDA, a computer, etc. In another application, target object 20' might be an occupant of the front passenger seat in a motor vehicle. System 10 can discern whether the occupant is an adult, a child, an infant, etc., even in strong ambient light. In such application, companion device 200 might be the control electronics for an air bag supplemental restraint system within the car. The control electronics can then intelligently deploy the air bag in one manner if the occupant to be protected is an adult, and can deploy differently if the occupant is a small child.

[00110] Although various embodiments of the present invention have been described in the context of dynamic range enhancement for three-dimensional image sensing, it is understood that embodiments of the present invention may be used in other applications that require dynamic range enhancement in the presence of a strong common mode signal. Further, those skilled in the art will appreciate that some or all of the described embodiments may be implemented with components other than the specific semiconductor switches, amplifiers, comparators, integrators, counters, etc. described herein.

[00111] The foregoing descriptions of specific embodiments of the present invention have been presented for purposes of illustration and description. They are not intended to be exhaustive or to limit the invention to the precise forms disclosed, and obviously many modifications and variations are possible in light of the above teaching. The embodiments were chosen and described in order to best explain the principles of the invention and its practical application, to thereby enable others skilled in the art to best utilize the invention and various embodiments with various modifications as are suited to the particular use contemplated. It is intended that the scope of the invention be defined by the Claims appended hereto and their equivalents.